Complementary Symmetry Nanowire Logic Circuits: Experimental Demonstrations and *in Silico* Optimizations

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ABSTRACT Complementary symmetry (CS) Boolean logic utilizes both p- and n-type field-effect transistors (FETs) so that an input logic voltage signal will turn one or more p- or n-type FETs on, while turning an equal number of n- or p-type FETs off. The voltage powering the circuit is prevented from having a direct pathway to ground, making the circuit energy efficient. CS circuits are thus attractive for nanowire logic, although they are challenging to implement. CS logic requires a relatively large number of FETs per logic gate, the output logic levels must be fully restored to the input logic voltage level, and the logic gates must exhibit high gain and robust noise margins. We report on CS logic circuits constructed from arrays of 16 nm wide silicon nanowires. Gates up to a complexity of an XOR gate (6 p-FETs and 6 n-FETs) containing multiple nanowires per transistor exhibit signal restoration and can drive other logic gates, implying that large scale logic can be implemented using nanowires. *In silico* modeling of CS inverters, using experimentally derived look-up tables of individual FET properties, is utilized to provide feedback for optimizing the device fabrication process. Based upon this feedback, CS inverters with a gain approaching 50 and robust noise margins are demonstrated. Single nanowire-based logic gates are also demonstrated, but are found to exhibit significant device-to-device fluctuations.

KEYWORDS: nanotechnology · complementary circuits · nanowire · field effect transistors · circuit simulations

The miniaturization of field-effect transistor (FET) circuits has prompted researchers to investigate new options for lithographically patterned structures, as well as new classes of devices, such as those that can be prepared using bottom-up fabrication techniques. Lithographically patterned options include bigate and trigate FET structures,[1] while nanowires (NWs) and nanotubes [2,3] comprise the bulk of materials that are being explored as bottom-up assembled alternatives.

Demonstrations of individual NW and nanotube devices, [1−3] as well as methods for organizing these building blocks into regular arrays have been reported.[4−6] Furthermore, as research into NW materials has moved forward, a variety of potential applications have been found that appear to be unique to NWs.[7−9] Nevertheless, variations in both device properties and assembly methods remain as outstanding problems for harnessing these materials for almost any application. As the numbers of unique NW applications rises, it becomes increasingly important to address these problems. For example, we and others have recently demonstrated that silicon NWs can serve as high efficiency thermoelectric materials.[10,11] Taking this specific example, if NWs are to find eventual use in thermocooling or thermopower applications, then conditions in which large numbers (and high packing densities) of both p- and n-type NWs can be reliably fabricated and harnessed within the same circuit are required.[12]

In this paper, we explore the use of very narrow (33 nm) pitch arrays of 16 nm wide Si NWs for complementary symmetry (CS) logic circuit applications. Our goal is not to compete with state-of-the-art CMOS type CS logic circuits such as can be fabricated from bigate and trigate FETs. In fact, the density of our NW array precludes such an effort, since there is not room in between adjacent NWs for a gate electrode to "wrap-around" the NWs—a characteristic that effectively defines bigate and trigate FETs. Instead, our goal is to demonstrate that high-density arrays of p- and n-type Si NWs can be harnessed to yield some of the demanding metrics that characterize CMOS logic. Those metrics, in turn, can guide the development of the Si NW arrays for nonlogic applications, since they require that certain, generic issues such as the establishment of ohmic contacts, spatial control over

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impurity dopants and dopant levels, signal routing, integration of p- and n-type FETs, etc., be addressed.

In particular, the metrics we focus on are signal gain (requires matching the performance of p- and n-type FETs), signal restoration (requires matching the logic gate input and output voltage-levels), signal cascading (requires one logic gate output to drive the input of a second gate), and operational noise margins (potentially permits robust circuit performance even when not all devices within a circuit perform ideally). We do not focus on device speed because most unique NW applications, such as thermoelectrics, sensors, photovoltaics,[13] etc., require relatively long NWs, but not high speed. However, we do focus on integrating statistical numbers of NW FETs into our circuits, since uniform performance across many NWs is a generally useful trait to achieve.

Complementary symmetry logic circuits utilize multiple p- and n-type FETs in order to achieve power efficiency. Predictable and matched FET performance is vital for signal restoration and cascading. We present architectures and performance metrics for several CS logic gates based upon 16 nm wide silicon NWs. All gates exhibit full signal restoration, and complexity up to an XOR gate (6 n-FETs and 6 p-FETs) is demonstrated. Nevertheless, the noise margins, gain, and energy efficiency of these logic gates are significantly inferior to existing CMOS technology. Thus, we explore the *in silico* optimization of the simplest CS logic circuit—the inverter. We utilize experimentally measured current−voltage and capacitance measurements of individual (long-channel length) NW p-FETs and n-FETs as inputs to a circuit simulator. The simulator faithfully reproduced those measured responses, and then allowed us to computationally explore alternative device concepts, such as separately optimizing the numbers of p- and n-type NWs per FET, or simulating the influence of different gate electrode materials on NW FET performance. These simulations suggest improvements in the device fabrication procedure, which are then implemented to prepare CS NW inverters with noise margins and signal gain that are significantly improved, and are comparable to existing CMOS devices. Finally, demonstrations of single NW-based CS logic gates are also presented. These gates exhibit inferior performance characteristics to the CS logic gates that involve multiple NWs per FET, and fundamental challenges associated with utilizing single NW-based CS logic gates are discussed.

Cross-bar structures[14] comprise a useful architecture for nanoscale memory[15] and logic circuits.[16,17] The crossbar can be tolerant of manufacturing defects because, if appropriately addressed, it possesses a built in redundancy. For memory, crossed NW junctions define the location of a memory bit. For the logic circuits discussed here, the bottom (horizontally oriented) wires are aligned arrays of p- and n-type Si NWs. The top (vertically oriented) wires are submicrometer wires. A nanowire/submicrometer wire crosspoint can be an ohmic contact, a gate electrode crossing the source-drain channel of a NW transistor, or a crossing of two electrically isolated wires.

For a CS logic gate, multiple p- and n-type NW FETs are required, and each must operate predictably and reliably. The NW FETs discussed here do exhibit such operation, and this is enabled by three nanofabrication techniques. First, the superlattice NW pattern transfer, or SNAP method,[18] can be harnessed to produce highly aligned and uniform arrays of Si NWs with excellent conductivity properties.[19] Second, signal routing between NW FETs within a given array may be achieved within the same single crystal (monolithic) Si epilayer film from which the NWs are formed.[20] This greatly minimizes the numbers of electrical contacts required. Finally, as previously reported, we utilize a diffusion-based doping technique that allows for the side-by-side production of p- and n-type doped Si NWs, and produces a sharp doping gradient through the NW, with the NW surface being the most highly doped.[21] This allows for heavily doped contact regions on the NWs and, by using those contacts as etch masks, the formation of lightly doped source-drain channels.

Figure 1 illustrates the full circuit fabrication process that combines the SNAP technique with patterned doping and monolithic contacts (for more information, see the Methods section).

RESULTS AND DISCUSSION

Complementary Symmetry Logic Gates with Multi-Nanowire FETs. In this paper we integrate these three approaches to fabricate members of the CS logic gate family, including NOT, AND, NAND, OR, NOR, and XOR. Three of these gates (AND, OR, and XOR) comprise multiple stages, with the output from one gate serving as a logic input to downstream circuitry. An important requirement of staged logic is signal restoration, that is, the output signal should be restored to the same level as the input in order to drive the next stage and thus ensure signal cascading. This means that the operational ranges of individual FETs must be matched.

The simplest single stage CS gate is the NOT gate, or inverter. We have previously reported on CS NW inverters.[21] For this discussion, they provide a good framework for discussing signal restoration and how it applies to multistage logic. A CS inverter contains one p-FET and one n-FET, with resistances R_p and R_n, respectively. The signal out from the inverter has a voltage value given by

$$V_n + (V_p - V_n)\frac{R_n}{R_p + R_n} \quad (1)$$

or

$$V_p - (V_p - V_n)\frac{R_p}{R_p + R_n} \quad (2)$$

where V_p and V_n represent the gate voltages that are required for placing the p- and n-FETs into their respective high conducting states. For obtaining full signal restoration V_n (V_p) should also fully turn a p-FET (n-FET) off. This is also critical for achieving energy efficient operation. Thus, for an input (top gate) range of V_{low} to V_{high}, V_p should equal V_{high}, and V_n should equal V_{low}. In practice, these voltage levels can fluctuate somewhat, and, within limits, the operational characteristics of the logic gates should be invariant to these fluctuations. The degree of this robustness is described by the noise margins (NMs). NM_{LOW} (NM_{HIGH}) is defined as the difference between the input and output voltages in their L (H) state at unity gain. Ideally, NM_{HIGH} and NM_{LOW} should both be large and matched to one another.

A second metric that is related to the noise margins is the gain: a gain <1 implies no NMs. Gain is defined as the maximum slope of the transition between the high (H) and low (L) voltage states. A greater than unity gain is required for full signal restoration, and a large gain implies better noise margins.

In general, V_{low} and V_{high}, for a given source-drain channel material and dopant profile, are determined by the gate dielectric and electrode materials. The conducting Si wafer that supports the SOI film can also influence these NW FETs. It was grounded for all measurements.

Although our n-FETs exhibit good current modulation (>1000), the off-current is non-negligible (~100nA) at $V_{GS} = 0$ V (for $V_{DS} = 1.5$ V). V_p does not fully turn our n-FETs off, thus limiting the efficiency of our logic gates. We will return to this discussion later (see Supporting Information for representative FET data). Our CS inverters all exhibited full signal restoration with a typical gain of 8. This gain represents an approximately 2-fold improvement over our earlier reports on NW inverters.

NAND and NOR gates require twice the number of FETs than what are needed for NOT gates, and thus are more sensitive to performance fluctuations of the component FETs. Nevertheless, signal restoration and positive gain characteristics were observed in all single stage logic gates. Results from a NOR gate are shown in Figure 2 and other results are included in the Supporting Information.

From Figure 2F, the NOR output is a logic 0 (−3 V) when either or both of the inputs are a logic 1 (0 V). The output is a logic 1 only when both inputs are 0. The output range is the same as that of the input, suggesting full signal restoration. The output switching characteristics when one input gate is held at 0 V and the second one is scanned from −3 to 0 V (Figure 2F, inset) reveal statistical variations of each individual FET. Nevertheless, there is an operational window where the logic gate performance is robust to such variations. A gain >1 was observed for all single-stage gates.

The results for the NAND and NOR gates suggests that the variations in our NW-based n- and p-FETS are small enough to permit the operation of staged CS logic gates. Figure 3 shows typical data that illustrates signal restoration for a Si NW-based CS AND gate (a NAND followed by a NOT). For these gates, when our p-FETs were operated with a drain-source voltage (V_{DS}) of −1.5 V, the p-FETs were turned on when $V_{low} = -3$ V and they were turned off for a V_{high} value of 0 V. We matched this performance by operating the n-FET within the effective range of 0 V and +3 V for $V_{DS\text{-}NFET} = 1.5$ V.

If the output of a NAND gate is utilized as the input of a NOT gate, AND functions are generated (Figure 3). For AND logic, only when the A and B inputs are logic 1, is the output a logic 1. If the signal at the output of stage 1 is not fully restored, however, the output of stage 2 will deviate noticeably from the high and low

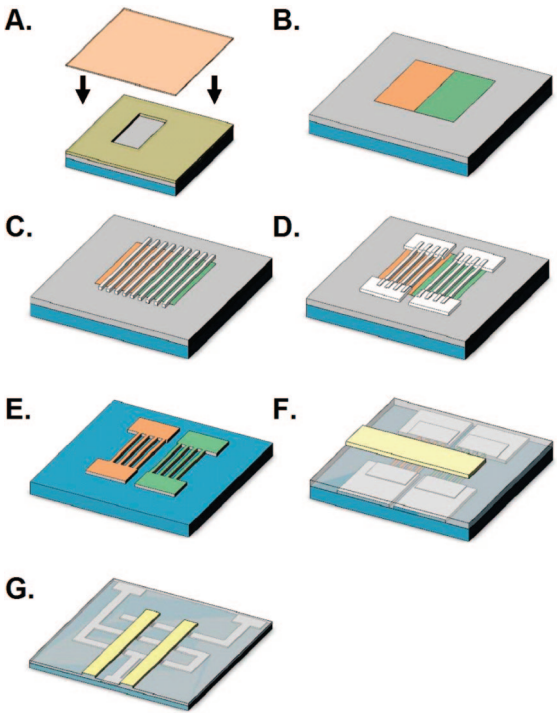

Figure 1. Schematic of the CS logic circuit fabrication process. (A) Regions of the SOI wafer are selectively p-type-doped by lithographically defining windows in an undoped spin-on lass film and coating the substrate with a p-type spin-on-dopant and annealing. (B) The process is repeated for n-type regions, generating n- and p-type patterned regions across the substrate. (C) The Pt NWs are formed via the SNAP process over the patterned doped regions. (D) Pt microware contacts are patterned over the NWs using electron beam lithography (EBL). (E) The NW and microwires are transferred into the silicon film, resulting in NWs contacted to larger pads, but all from the same single crystal silicon epilayer. (F) The device is patterned with metal source and drain contacts, an Al_2O_3 gate dielectric and then metal gate electrodes using EBL. (G) Steps A−F are done simultaneously on multiple sections of the n- and p-type NWs to generate multiple copies of each of the CS logic circuits discussed here.

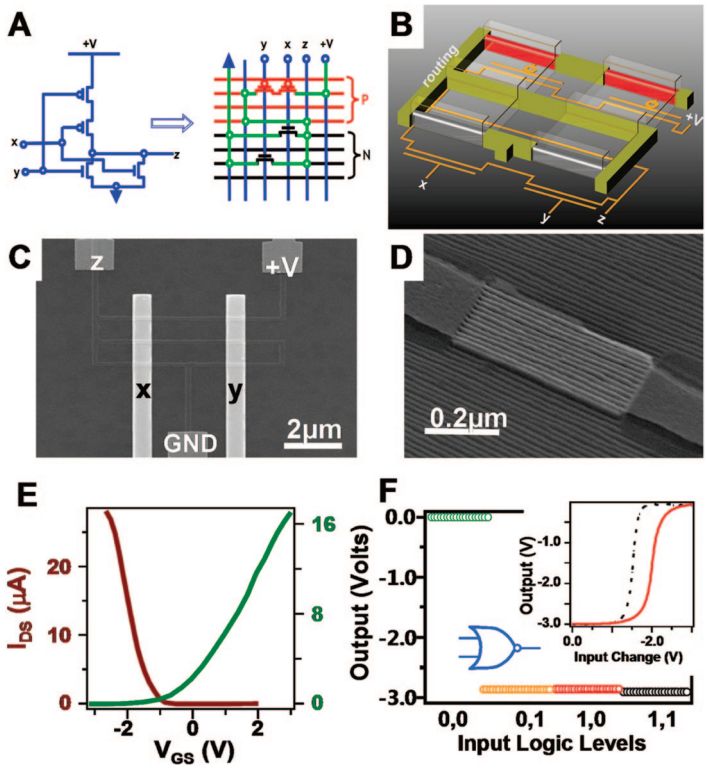

Figure 2. Complementary symmetry nanowire logic circuits. (A) Implementation of logic gate in an ultrahigh density nanowire array using the crossbar scheme. The equivalent circuit diagram is shown on the left. (B) A perspective cartoon picture of a NOR gate with monolithic contacts. Red and gray blocks represent p- and n-type nanowires, respectively, and the green blocks are monolithic routing wires. (C) Top view SEM picture of an actual NOR gate. Visible in this picture are only routing wires because of the low magnification. The metal contact pads for power supply and ground and the two input wires are in different layers (separated by Al_2O_3 dielectrics). (D) A blow up of the monolithic contact of the routing wires to the nanowire array. This picture was taken prior to Al_2O_3 deposition for clarity. (E) Typical S/D current plot *versus* gate voltage for both p- ($V_{DS} = -1.5$ V) and n-FETs ($V_{DS} = 1.5$ V). Note that the p-FET current has been multiplied by −1 for plotting on the same range as with the n-FET. (F) A NOR gate truth table is reproduced. Low output = −3 V, high = 0 V. The inset shows the switching characteristics when one input is held constant and the other input is swept from 0 V ("1") to −3 V ("0"). The solid and broken traces are of the output as an individual input is swept.

logic levels. OR gates are fabricated similarly (Supporting Information).

The most complicated two-input binary logic gate is the XOR gate, which outputs a logic 1 when one and only one of the inputs is a logic 1. A 2 bit half a dder, for example, involves an XOR gate to sum the two binary numbers and an AND gate to calculate the carry. The AND and OR gates demonstrated above can be approximated by linear functions and, in fact, both of these types of logic gates can be generated by linear circuit elements using an approach known as resistor or diode logic.[22] In other words, as the input logic values increase from 00 to 01 to 10 to 11, the output varies from high to low, or from low to high. For an XOR gate, as the input logic value increases, the output varies from low to high and then back to low; that is, the XOR gate is intrinsically a nonlinear function. It is not surprising, then, that the XOR gate is a significantly

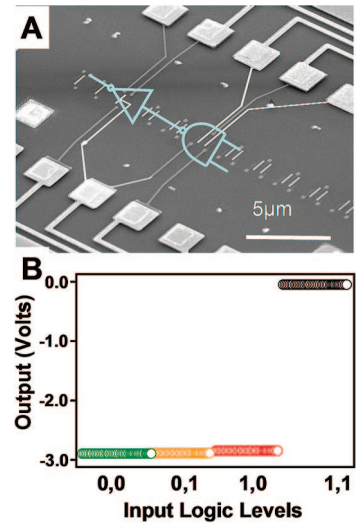

Figure 3. (A) Complementary symmetry 2-stage AND gate, composed by a NAND gate and a NOT gate (inverter), as indicated in the electron micrograph. (B) The measured truth table of this AND gate, indicating full signal restoration. A "1" is 0 V and "0" is −3 V.

more complex circuit. A CS XOR gate requires 6 p-FETs and 6 n-FETs. Two NW CS inverters are first utilized to create complementary inputs $\bar{A}$ and $\bar{B}$ from inputs A and B. All four of these logic values then serve to drive a circuit of 8 NW FETs, with each input utilized to drive a p-FET and an n-FET.

The XOR gate equivalent circuit is shown in Figure 4. A SEM micrograph of the actual device is shown in the Supporting Information. When all 12 FETs operate consistently, a functional XOR gate is achieved. Without the nanofabrication advances that allowed us to construct highly doped, NW-to-NW signal routing pathways within the same single crystal Si epilayer from which the NWs are formed, it is unlikely that the NW CS XOR gate would achieved full signal restoration.

Our yield of working n- and p-FETs was likely near 100%. However, the requirement that the NW n- and p-FETs be well matched with each other so that a CS logic gate will exhibit full signal restoration is a very stringent one. We tested 15 XOR gates and found that only 5 exhibited full signal restoration. If a single NW FET within an XOR gate performed out-of-range, the XOR gate would fail, and this is likely the dominant failure mode. There were 180 FETs tested in the 15 XOR

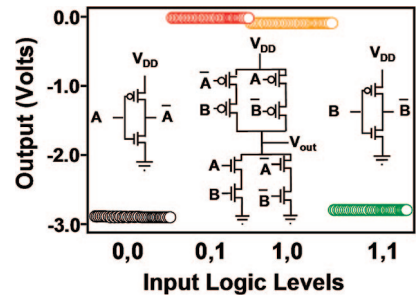

Figure 4. The truth table of a nonlinear 2-stage gate, XOR, whose equivalent circuit diagram is shown in the inset.

gates, and the 33% yield in XOR gates implies an approximately 93% yield in working and matched FETs.

In Silico Simulations of Device Performance. The CS logic gates discussed above worked, but only for a limited range of operational parameters (i.e., the combination of V_{SD}, V_{low} and V_{high} values). This limited range will ultimately limit the yield and performance of large-scale CS NW logic circuits. An attractive approach toward improving the performance and yield of NW CS logic gates is to explore different device architectures that can broaden the operational definition of "well-matched FETs". This means finding ways to better match the noise margins and to improve the other performance metrics (such as reducing the ~100 nA leakage currents observed) of the p- and n-FETs. The experimental possibilities for improving the operational characteristics of the individual FETs are vast and include the nature and quality of the gate dielectric, the gate electrode material, the source-drain channel length, and numbers of NWs utilized per FET, etc. Thus, we turned to computer simulations for guidance to further improvements.

Taking inverters as the prototype for NW CS logic gates, we explored *in silico* methods toward further optimizing those devices, and tested those results by fabricating a new generation of CS NW inverters. Computer-aided design (CAD) simulation tools can increase the efficiency of electronic circuit optimization by yielding insights into circuit performance and providing feedback for improved fabrication. NW and CNT devices have been modeled in a circuit simulation environment,[15−17] although those efforts have largely neglected the fabrication and materials challenges of associated nanocircuits. The addition of CAD simulation tools into the nanocircuit design process permits a broad exploration of fabrication space, without the associated time and expense of having to physically make the actual devices. It can thus provide a very efficient pathway toward guiding that optimization of NW circuit performance.

We utilized data-driven circuit simulations, focusing on a few of the key CMOS logic performance metrics that could be represented by a NW CS inverter.[23] From candidate Si NW FETs, current−voltage ($I-V$), conductance−voltage ($G-V$), and capacitance−voltage ($C-V$) data were tabulated and introduced into the circuit simulation environment. We then investigated, *in silico*, a variety of circuit metrics for a CS inverter, with a focus on optimizing gain and noise margins.

NW FET test structures were formed from arrays of Si NWs at 33 nm pitch. The FET structures were similar to the multi-NW p- and n-FETs described in the previous section, except the transistor channel dimensions under the gate were 12-μm wide, contacting 400 NWs, and 9−11 μm long.[23,24] Such large test structures were required to obtain high quality and reproducible

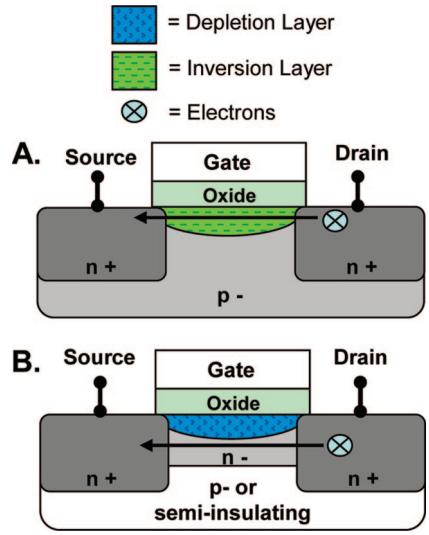

Figure 5. Comparison of conventional MOSFET to buried-channel (BC) MOSFET structures. (A) Conventional MOSFET structure, operating in inversion mode. Carrier conduction occurs at the surface of the channel. (B) BC-MOSFET structure. The gate creates a depletion region in the channel and conduction occurs away from the surface.

capacitance-voltage measurements. The NW arrays were contacted with Ti/Pt source/drain electrodes and were patterned with a Ti/Pt top gate above a 10-nm thick Al_2O_3 dielectric layer.

The threshold voltage (V_T) for the NW FET test structures was calculated from the experimentally obtained $I_{DS}-V_{GS}$ plots. Our NW FETs are similar to buried-channel MOSFETs (BC-MOSFETs), where the conduction is modulated by controlling the depth of a depletion region, rather than an inversion layer, as in a typical MOSFET (Figure 5).[25] In a BC-MOSFET, the conduction path is below the gate-induced depletion region, leading to a higher mobility relative to MOSFETs, since surface scattering is reduced. There are two V_T values to consider: the voltage where the channel is completely depleted and voltage at the onset of surface conduction, where the gate no longer controls the buried-channel.[25,26] This latter V_T is more comparable to V_T of conventional MOSFETs and so will be presented in this paper.

$V_{GS} < V_T$ defines the subthreshold region. In BC-MOSFETs, conduction is due to partially depleted carriers in the channel, not the formation of a weak inversion layer. However, for both BC-MOSFETs and conventional MOSFETs, the current is an exponential function of V_{GS},[27] and so the subthreshold swing can be calculated using equivalent techniques.[28]

V_T values were calculated by fitting the linear region of the $I_{DS}-V_{GS}$ curves and extrapolating to $I_{DS} = 0$ at low (100 mV) drain bias. This is approximated by the simple model,

$$I_{DS} = \mu_{eff} V_{DS} (W/L) C_{OX} (V_{GS} - V_{TLIN} - V_{DS}/2) \quad (3)$$

Here, μ_{eff} is the effective channel mobility, C_{OX} is the gate oxide capacitance, and V_{TLIN} is the linear threshold voltage. Equation (3) holds when $V_{GS} - V_{TLIN} > V_{DS}$.[29] The linear region was determined by fitting to the slope around the voltage at maximum transconductance, g_m. Once V_T was found, the subthreshold swing, **S**, (or inverse subthreshold slope) could be determined by fitting a line to the linear portion of the $\log(I_{DS}) - V_{GS}$ plot at $V_{GS} < V_T$. This method for determining **S** is different (and produces a higher value) than what has been reported by various groups, including us, for NW or CNT FETs,[18,24,25] but yields results more comparable to standard MOSFET parameters.

For n-type NW FET test structure, V_T and **S** were calculated to be −0.9 V and ~550 mV/dec, respectively. For the p-type NW FET test structure, the values were −2.3 V and ~450 mV/dec. For BC-MOSFETs, the ideal value for **S** is >80 mV/dec. As the channel thickness increases relative to the substrate, **S** becomes >100 mV/dec. In our NW devices, there is no substrate junction to help modulate a depletion region, and the gate only modulates the top of the NWs, leading to a reduction in **S**.[30] Other issues, such as surface states, and the thick (and low-quality) gate dielectric contribute to a larger **S**. However, these devices still exhibit excellent on/off ratios (approximately 10^4 for both p- and n-FETs) and high on-currents (p-type, ~1 μA; n-type, ~5 μA).

Simulation Methodology: DC Analyses. Device look-up table models, typically derived from analytical device models, have been implemented using several simulators, including SPICE.[27−30] Tabular models are typically utilized to decrease the computation time of complex simulations. Here, we employed tabular models to rapidly evaluate prototype device designs. Complete NW FET $I-V$, $G-V$, and $C-V$ measurements were compiled into a look-up table for access by the circuit simulator, which maps each I, G, and C value for a given set of gate and source-drain voltages (at 100 mV increments) as a point within a uniform grid. The device data is thus used to create the complete model; no additional models or fitting parameters are needed for accurate solutions. This method requires high quality $I-V$, $G-V$, and $C-V$ measurements, which are readily achieved using SNAP NW devices due to the highly uniform quality of the SNAP NWs. The accuracy of the look-up table is validated by recreating the test structure transistor curves (with a low simulation error of ~0.1%) using the simulator, shown in Figure 6.

The DC analysis capabilities of this model were tested using a CS inverter (Figure 7A). The power supply for this circuit, V_{DD}, is at +4 V. The gain of the simulated inverter (~4) is comparable to previously published devices but about a factor of 2 worse than the circuits fabricated in the previous section.[21] The gain of the simulated inverter was <1 at the input L state, and so NMs could not be calculated. The inverter does not fully regenerate signal to +4 V at the input L state (indicated by a red arrow on Figure 6A). Since the output is lower than V_{DD}, the n-FET is not fully "off", resulting in a high leakage current of 3 μA at the input L state. Also, the center of the inverter curve is shifted toward the input L state, indicating the n-FET has a larger saturation current than the p-FET. These reduced performance metrics likely are because the geometry of these devices were optimized for obtaining reliable $C-V$ data.

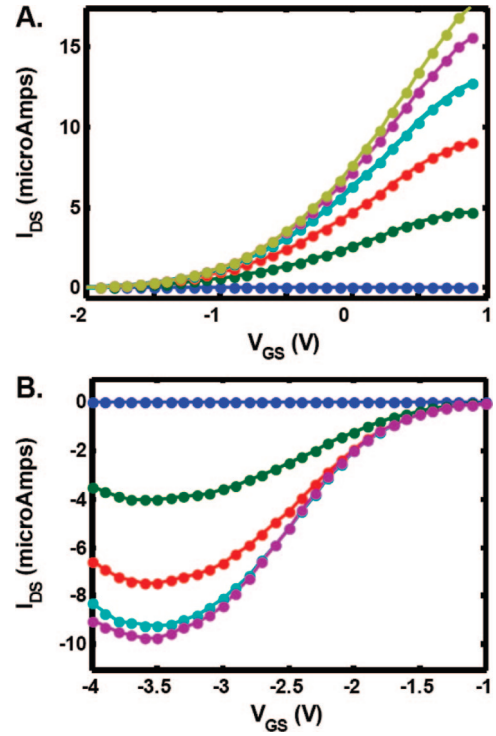

Figure 6. Comparison of simulated (solid lines) and experimental (solid circles) device parameters. (A) N-FET data for drain-to-source current (I_{DS}) versus gate-to-source voltage (V_{GS}) for drain to source voltages (V_{DS}) of 0 V (blue) to + 2.5 V (gold). The error between simulated and experimental values is approximately 0.1%. (B) Analogous curves for p-FETs for V_{DS} of 0 V (blue) to −2 V (purple).

Simulating a V_T shift for the n-FET in the circuit and better matching the current levels between two FETs generates an improved inverter curve (Figure 7B). A battery element that offsets the input voltage (a −0.8 V shift relative to the original V_T was optimal) for the n-FET was incorporated into the simulation to shift V_T. In addition, saturation current levels were improved by scaling the number of NWs per device to 10:1 (p-FET:n-FET). This is analogous to the size scaling of MOSFETs in CMOS digital circuits, which is typically done to compensate for the difference of hole and electron mobilities.[31] The resulting simulated inverter is fully regenerative and has a gain of ~45, with large, well matched NMs of 1.2 and 1.4 V. The curve is symmetric over $V_{DD}/2$, indicating current matched devices. The leakage current also improved to 14 nA at the input L state − this leakage current represents approximately an order of magnitude improvement over what was observed for

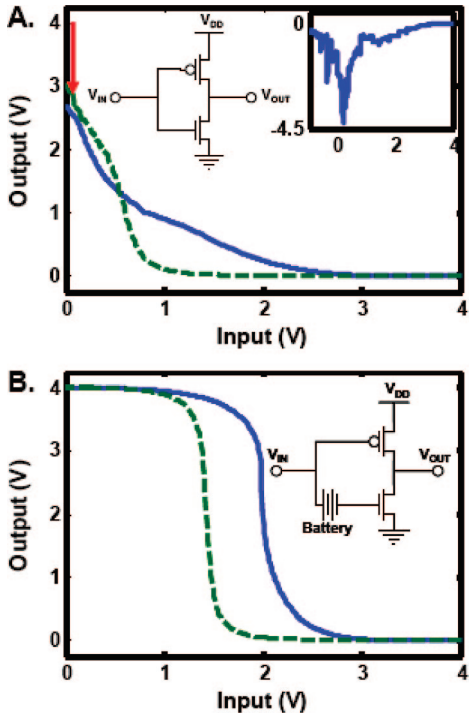

Figure 7. Simulated and experimental dc voltage characteristics of initial and optimized CS inverter. (A) Input *vs* output voltages of initial simulated (solid blue line) and fabricated (dashed green line) inverter. The red arrow indicates where the output voltage is not restoring to the power supply, V_{DD}. (Left inset) Circuit schematic of CS inverter; (right inset) simulated inverter gain as a function of input voltage. (B) Inverter characteristics of simulated (solid blue line) and fabricated (dashed green line) optimized inverter. (Inset) Circuit schematic of inverter with additional battery element. The fabricated device approximated this circuit through the use of separate power supplies for the p- and n-FETs.

the optimized CS logic gates discussed above. These results show that by shifting the V_T on the n-type NW FET and scaling the device widths to match their saturation currents, the inverter characteristics are significantly improved.

Experimental Verification of Simulated Predictions. Figure 7A (dashed green line) shows the original experimentally measured inverter DC transfer characteristics. This curve has many similar characteristics to the predicted inverter curve. The measured inverter has a comparable gain (~7.5) and NMs also could not be calculated. It also lacks signal restoration at the input L state, and is not symmetric over $V_{DD}/2$.

We introduced an additional power supply for separately driving the n- and p-FETs in analogy to the simulated battery element. With an input voltage shift of −800 mV on the n-FET, the inverter exhibited full signal restoration, NMs of 2.1 V (H) and 1 V (L), and a gain of ~30 (Figure 7B, dashed green curve). The voltage swing shifted to the left because of the mismatched current levels of the n- and p-FETs, which was corrected in the simulations. Otherwise, the curves are in good agreement with each other.

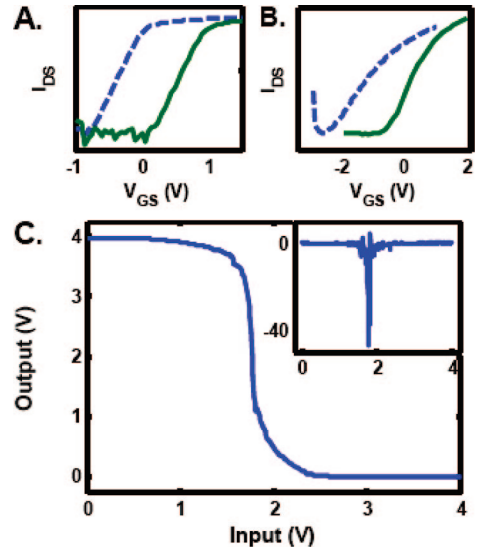

Figure 8. Comparing different gate electrode metals for n-FET devices and resulting inverter characteristics. (A) Semilog plot of I_{DS} *vs* V_{GS} for MEDICI modeled structure with Ti gate metal (dashed blue line) and Pt gate metal (solid green line). (B) Experimentally obtained semilog I_{DS} *vs* V_{GS}, comparing of Ti gate (dashed blue line) *vs* Pt gate (solid green line) metal for fabricated NW structures. (C) Input vs output voltage characteristics of fabricated CS inverter with Pt-gate n-FET. (Inset) Inverter gain.

Introducing additional power supplies into the inverter circuit simulation (Figure 7B) highlights the need to shift the n-FET V_T. Obviously introducing a battery element into the circuit is unrealistic; however, utilizing different gate electrode materials for the n-FETs and the p-FETs can accomplish the same goal. A gate metal with a higher work function, Φ_M, relative to the electron affinity of the n-type Si, will promote a large depletion region at $V_{GS} = 0$ due to band bending at the metal-oxide−Si interface. MEDICI (Synopsys, Inc.), a 2D semiconductor device simulator, was used to confirm that this effect would be large enough to make $V_T > 0$ (see the Supporting Information for details).

For channel doping $<10^{18}$ cm^{-3}, a large V_T shift was observed for the n-FET device, in both the MEDICI simulations (Figure 8A) and experimentally (Figure 8B) by replacing the Ti gate metal ($\Phi_M = 4.28$ eV) with Pt (5.6 eV). This effect was observed in both the modeled and fabricated structures for low-doped channels only; dopant concentrations $>10^{18}$ cm^{-3} do not facilitate the formation of a large depletion layer (see Supporting Information). From the circuit simulation results, the S/D contacts were also patterned so that the n-type devices were narrower (0.75−1 μm wide, contacting ~22 to 30 NWs) to achieve the matched saturation currents (~15:1 p-FET/n-FET width).

Several of the Pt gate n-FETs were paired with the p-FETs to form CS inverters (Figure 8C). The gain of the inverter circuit increases to ~45, with well matched NMs of 1.2 and 1.5 V. All of the tested circuits had gains >15 and showed full signal restoration. This dramatic

improvement over the original devices was consistent with the DC simulated predictions.

Simulation Methodology: Transient Analyses. The inverter transient characteristics were briefly investigated by calculating the circuit's propagation, or gate, delay, t_{pd}. This constitutes the time difference between the midpoint of the input swing and the midpoint of the output swing, and can be used to estimate the speed of complex circuits.[32] Propagation delay can be calculated from:

$$t_{pd} = \frac{C_L \cdot V_{DD}}{2I_{D(SAT)}} \quad (4)$$

where C_L is the load capacitance and $I_{D(SAT)}$ is the saturation current for the FET. To measure the propagation delay, the inverter circuit was designed using a second inverter as the load capacitance (see Supporting Information for details). Since the measured gate capacitance is ~0.35 pF for one device, the total load capacitance is ~0.7 pF, ignoring any wiring capacitance. $V_{DD} = +4$ V for this circuit and the saturation currents for the n-FET and the p-FET are 9 and 100 μA, respectively. This leads to a calculated $t_{dr} = 160$ ns and a $t_{df} = 14$ ns. The same inverter circuit with C_L was also examined in the simulation environment. The simulated propagation delay values are $t_{dr} = 180$ ns and a $t_{df} = 20$ ns. The good agreement between the simulated and calculated delay values demonstrates the accuracy of the tabular model-based simulations for transient metrics. The implication is that these simulation methods could also be utilized to optimize device speed.

Scaling CS Logic Gates to Single Nanowire Devices. All building block FETs discussed above involved 5−10 NWs or more. This is because FETs of this size (~250 nm wide) are not only easily fabricated, but p-FETs with relatively large numbers of NWs were required to current match the NW n-FETs. Nevertheless, single NW FETs do represent a limit in terms of FET size, and so we explore those here. Single NW devices would be expected to be characterized by very significant device-to-device deviations. Consider, for example, a 20 nm tall, 15 nm wide, 300 nm long source-drain channel. At a doping level of 10^{17} (a typical doping level for a bulk Si FET) there are only about 10 dopant atoms within the channel. Thus, even small fluctuations in the physical properties of the NWs may lead to very large fluctuations in their performance metrics.[33] This has been pointed out as a potentially fundamental issue that can ultimately limit the size scaling of Si circuits.[34]

We fabricated a number of single-NW devices. As with the multiwire devices, we fabricated monolithic contacts so that the single NWs were connected to large pads constructed from the same single crystal silicon sheet. We characterized both the single-NW-based FETs and single-NW-based logic gates. Forming single-NW FETs with monolithic contacts is similar to

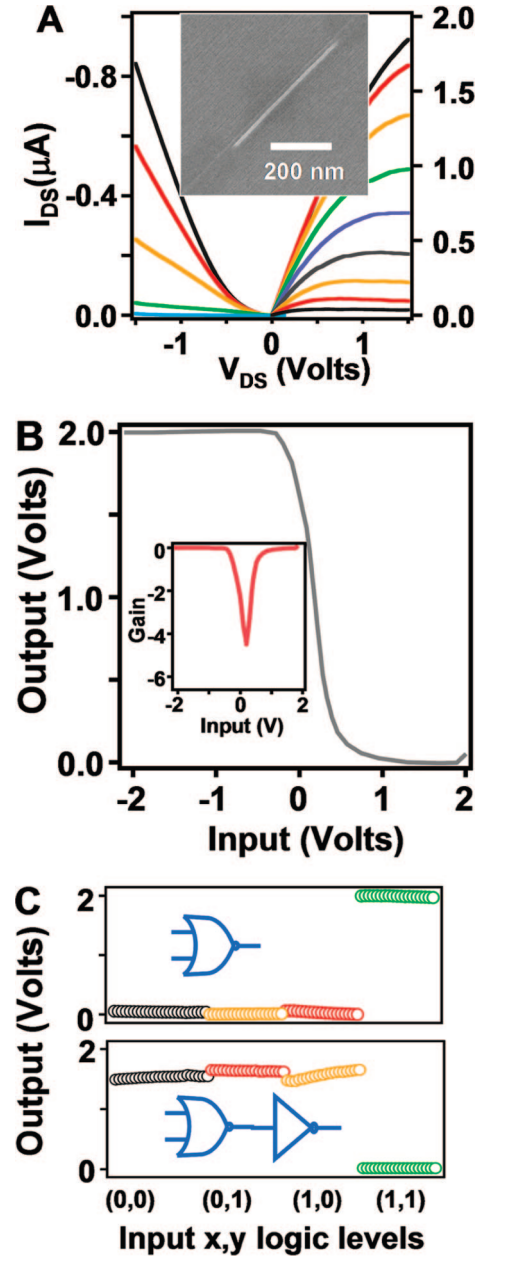

Figure 9. Single NW logic gates. The characteristic building-block FET performance is shown in panel A, with both p- (left) and n-FETs (right) combined. V_{GS} values are varied from −2 to 2 V for p-FETs in 1 V interval and 2 to −2 V for n-FET with 0.5 V interval. (B) a CS inverter is built upon single NW FETs, with the inset showing gain *vs* input plot. (C) CS NOR (above) and OR (below) gates built on single NW devices, with the traces corresponding to the indicated input logic levels.

that of multiple-NW FETs except that the alignment requirement for the former is far more challenging. The electronic properties of complementary single-NW FETs were comparable to that of the multiple-NW ones (Figure 9A), with a few caveats discussed below. Inverters with gain ~4−5 (Figure 9B) were also obtained on seven of the eight tested devices. NOR and OR gates were also successfully demonstrated (Figure 9C).

There were a few key differences between single-NW devices and logic gates. Primarily, the

single-NW FETs exhibited larger variations from device to device (see Supporting Information for statistics). This could arise from intrinsic issues such as fluctuations in the numbers of dopant atoms or from variations in the surfaces of the NWs. Whatever the cause, because of these variations, our attempts to build multistage single NW-based logic gates with full signal restoration were not fully successful (Figure 8B). The output of the two-stage OR gate deviates significantly from that of the single-stage NOR gate (Figure 9C). These variations may be intrinsic to devices at this scale. If so, then novel device engineering, surface chemistries, etc. will almost certainly be necessary to construct reliable digital logic gates at extreme patterning densities and FET dimensions.[35,36]

CONCLUSIONS

We have demonstrated complementary symmetry logic gates from 16 nm wide p- and n-type Si nanowires. The logic gates exhibit full signal restoration, allowing for the demonstration of staged logic, in which the output of one stage drives the input of another, and staged logic gates containing as many as a dozen FETs were demonstrated. As fabricated, however, the logic gates exhibited a high leakage current and poorly matched noise margins between the n- and p-FETs. In silico simulations of complementary symmetry inverters indicated that the circuits could be significantly improved by varying the relative numbers of nanowires in the p-FETs and n-FETs, and by shifting the relative threshold voltages. This was attempted experimentally, with gate electrode materials varied between the n- and p-FETs so as to shift the relative threshold voltages. The resulting inverters exhibited a gain approaching 50 and well matched noise margins. For these two parameters, the nanowire inverters performed at a level comparable to existing CMOS technology. The viability of single nanowire-based complementary symmetry logic was also explored. NOT gates exhibiting a reasonable gain were demonstrated, but signal restoration sufficient to fully drive staged logic gates was not achieved. This limitation highlights the need to find alternative doping strategies that can be harnessed to limit the variable behavior observed in single-NW FETs. Nevertheless, many applications that require p- and n-type nanowires actually require statistical numbers of nanowires per device,[12] and the multi-NW FET-based CS logic gates that are reported here can provide a foundation for those applications.

METHODS

Fabrication of Logic Gates. In a typical fabrication process, an array of 400 Pt NWs were first formed on a SOI substrate with predefined doping patterns. Lithography was then carried out to define routing wires, followed by Pt deposition (10 nm) and liftoff. The entire pattern was finally transferred into the underlying SOI substrate *via* a directional reactive ion etching (details described elsewhere).[20] The resulting structure consists of high density NWs connected by Si routing bars, all in the same single crystalline layer. External metal contact pads were then formed to connect the Si routing bars, as shown in Figure 1. The devices were measured using the bottom gate for initial device assessment. Windows exposing the source-drain regions of the NWs were opened for selective etching to thin the NWs and thus adjust the doping level for optimized field-effect gate responses for p- and n-FETs. Once the desired electrical properties were obtained (on/off ratios $>$ 1000), a 10 nm Al_2O_3 gate dielectrice was formed by evaporating Al in an O_2 atmosphere (pressure $\sim 10^{-5}$ Torr) and Ti/Pt (50/20 nm) as top gate input wires were deposited. To enable probing of the devices, windows were opened over the measurement pads ($\sim$125 μm $\times$ 125 μm), followed by dry etching in BCl_3 plasma (flow rate = 10 sccm, pressure = 4 mTorr, power = 200 W) for 12 min to remove the Al_2O_3 dielectric. The fabrication was finally concluded by the deposition of a Ti/Au (10/50 nm) cap layer on top of the etched windows. The same etching recipe was employed for forming connections for the multistage logic gates (AND, OR, and XOR).

Large Area NW FETs. Si NW devices were fabricated on SIMOX-SOI wafers (34-nm $<$100$>$ Si on 250-nm Si oxide) (Simgui, Shanghai, China). Substrates were cleaned using the standard RCA process and then doped either n- or p-type by applying a spin-on-dopant (SOD) and annealing using rapid thermal processing (RTP). Immersion in a 6:1 NH_4:HF buffered oxide etch (BOE) removed the SOD postanneal. Four-point resistivity measurements confirmed the dopant concentration. The SNAP method was used to form the Si NW arrays on the prepared substrates. Portions of the Si NWs were selectively removed using a SF_6 plasma, leaving behind 20-μm long NW sections. S/D contacts were patterned using electron beam lithography (EBL), and Ti/Pt (40/20 nm) was deposited using an electron-beam metal deposition system. For the large area devices, the S/D contacts were patterned to be 12-μm wide to contact all 400 NWs with a 9$-$11 μm channel length. In the small area, Pt gate n-FET devices, the contacts ranged from 100 nm to 2 μm wide (only the 0.75 μm and 1 μm wide devices, contacting $\sim$22 to 30 NWs, were used in the inverter circuits) with 2 μm channel lengths. After the S/D contract electrode formation, all devices were annealed at 475 °C for 5 min in forming gas (95% N_2 5% H_2). Back-gated $I_{DS}-V_{GS}$ measurements were obtained using the Si substrate as the back-gate electrode. For the n-type devices, the channel was selectively thinned using a directional CF_4 plasma etch until the back-gate on/off ratio improved to $>$10. For all devices, 10-nm thick Al_2O_3 was deposited onto the device substrate. The top gate was formed over the entire channel length using Ti/Pt (40/20 nm) (large area n- and p-FET devices) or Pt (50-nm) (final n-FET devices).

Device Characterization. For the table look-up model, $I-V$ and $G-V$ data were collected using an Agilent B1500A Semiconductor Parameter Analyzer (Agilent Technologies) and C$-$V data werre collected with a HP 4284 LCR meter (Hewlett-Packard Company). The inverter circuits were controlled and measured with three Keithley 2400 SourceMeters (Keithley Instruments, Inc.). All devices were measured in probe stations using probe tips to contact the devices.

Modeling and Simulation. Circuit simulations were performed using the proprietary Intel Circuit Simulator in a UNIX environment. Device simulations were carried out using MEDICI (Synopsys, Inc.). Details on the structure and methods used for the MEDICI simulations can be found in the Supporting Information.

Single-NW Devices. Similar to a typical multi-NW device fabrication, the SNAP procedure, followed by the monolithic routing technique, were carried out to define basic device structures. The monolithic routing wires were patterned to be approximately $\sim$50 nm wide so that no more than 2 NWs were connected by one route. Afterward, a thin ($\sim$30 nm) Al wire was formed as a

sacrificial layer to protect the active NW and selective etching in CF_4 was utilized to remove unwanted NWs. Finally, the Al wire was removed in Al etchant (H_3PO_4:H_2O:HNO_3:CH_3COOH vt 16:2:1:1). To ensure good alignment between routing wires with Al sacrificial ones, the process was typically done in two steps. The first step was to form a layer of Al wires as alignment test. During this step, Al wires were formed and their relative locations with regard to routing wires were carefully measured. If they were misaligned, the error was recorded. This record was then utilized to make another layer of Al wires that were well aligned to routing wires after the removal of the test layer. It was found that after this two-step process, excellent alignment (less than 10 nm error) can be reliably achieved. Al_2O_3 gate dielectric and gate formation were identical to other logic gates.

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Supporting Information Available: This material includes additional discussion and figures on the circuit characteristics of the NOR, AND, OR, and XOR NW logic gates, the calculation of V_T and **S**, the MEDICI simulations, the effect of channel doping, and the transient analysis results. This information is available free of charge *via* the Internet at http://pubs.acs.org.

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